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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/739,758	12/20/2000	Takao Watanabe	HIT 2 482-06	7380

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EXAMINER
HIRL, JOSEPH P

ART UNIT	PAPER NUMBER
2121	7

DATE MAILED: 04/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,758	WATANABE ET AL.	
	Examiner	Art Unit	
	Joseph P. Hirl	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 25-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 25-32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 01 June 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 4,5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Wilbert L. Starks, Jr.
Primary Examiner
Art Unit - 2121

DETAILED ACTION

1. Claims 1-24 are cancelled. Claims 25-32 are new. Claims 25-32 are pending in this application.

2. The claims and only the claims form the metes and bounds of the invention. The Examiner has full latitude to interpret each claim in the broadest reasonable sense. Examiner will reference prior art using terminology familiar to one of ordinary skill in the art. Such an approach is broad in concept and can be either explicit or implicit in meaning.

Information Disclosure Statement

3. The information disclosure statement filed *December 20, 2000 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Drawings

4. Drawings 1-25 were used in application 09/198,658 which became U.S. Patent 6,205,556. Consequently, these drawings are prior art to the instant application and should be cancelled or labeled as "Prior Art." (MPEP 608.02(g).

Abstract

5. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The abstract submitted has 246 words.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 29 and 30 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The concepts of a "first memory array", "a second memory array", "a first signal path" and "a second signal path" were not established in the methodology of the specification.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Claims 25-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Mashiko (U. S. Patent 4,988,891 referred to as **Mashiko**).

Claim 25

Mashiko anticipates a memory array having a plurality of word lines, a plurality of bit lines, and a plurality of memory cells (**Mashiko**, col 1, lines 17-34; col 4, lines 17-24; col 3, lines 52-61); a processing circuit coupled to said memory array via a plurality of signal lines (**Mashiko**, col 2, lines 42-56); an input/output circuit coupled to one of the plurality of signal lines (**Mashiko**, col 5,

lines 27-59); and a switching circuit inserted between the plurality of signal lines and said input/output circuit (**Mashiko**, col 3, lines 38-51).

Claim 26

Mashiko anticipates input/output circuit is for inputting and outputting data from and to outside of said semiconductor chip (**Mashiko**, col 2, lines 37-67; col 3, lines 1-6).

Claim 27, 28

Mashiko anticipates each of the plurality of memory cells includes a MOS transistor and a capacitor, and wherein said processing circuit is formed by MOS transistors (**Mashiko**, col 15, lines 53-67; Examiner's Note (EN): Fig. 1 is a representation of a neuron. Fig. 4 is a schematic of a neural network. Column 4, lines 17-24 identify the transition from the neuron to the neural network. Neural networks have memory that resides in the network...weights and interconnectivity. The circuit implementation of figure 4 uses electronic solid state components to achieve the VLSI configuration of column 2, lines 37-41. Mashiko implements his invention using Metal Oxide Semiconductors (MOS) and other generic electronic components such as capacitors such as those components identified in column 15, lines 42-52).

Claim 29

Mashiko anticipates a first memory array including a plurality of DRAM memory cells (**Mashiko**, col 3, lines 52-61; EN: DRAM is dynamic RAM which is random access memory); a logic circuit coupled to said first memory array, said

logic circuit being formed by MOS transistors (**Mashiko**, col 2, lines 42-56; EN: row decoders, bit decoders, registers have logic circuits of a plurality degree implemented with generic MOS transistors); an input/output circuit coupled to said first memory array, said input/output circuit having nodes to and from which data is input and output outside of said semiconductor chip (**Mashiko**, col 5, lines 27-67; col 2, lines 37-56); a first signal path coupled between said first memory array and said logic circuit (**Mashiko**, col 2, lines 37-67); and a second signal path coupled between said first memory array and said input/output circuit (**Mashiko**, col 2, lines 37-67; EN: Mashiko references extensive coupling as is evidenced by Fig. 4. Digital circuits operate using logic circuits).

Claim 30

Mashiko anticipates a second memory array including a plurality of DRAM memory cells coupled to said logic circuit and said input/output circuit (**Mashiko**, col 2, lines 37-67; col 3, lines 52-61).

Claims 31 and 32

Mashiko anticipates each of the plurality of DRAM memory cells includes a MOS transistor and a capacitor (**Mashiko**, col 2, lines 37-67; col 3, lines 52-61; EN: above comments apply).

Conclusion

8. Claims 25-32 are rejected.

Correspondence Information

Any inquiry concerning this information or related to the subject disclosure should be directed to the Examiner, Joseph P. Hirl, whose telephone number is (703) 305-1668. The Examiner can be reached on Monday – Thursday from 6:00 a.m. to 4:30 p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, John Follansbee can be reached at (703) 305-8498. Any response to this office action should be mailed to:

Commissioner of Patents and Trademarks,

Washington, D. C. 20231;

or faxed to:

(703) 746-7239 (for formal communications intended for entry);

or faxed to:

(703) 746-7240 (for informal or draft communications with notation of "Proposed" or "Draft").

Hand-delivered responses should be brought to:

Receptionist, Crystal Park II

2121 Crystal Drive,

Arlington, Virginia.

Joseph P. Hirl

April 9, 2003

Wilbert L. Starks, Jr.
Primary Examiner
Art Unit - 2121